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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
CHU, GABRIEL L	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,579	NAIR ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-22* is/are allowed.

6)☒ Claim(s) *2-5 and 23-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claims 2-5 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6499048 to Williams.** Referring to claims 3, 4, Williams discloses a method of multithread processing on a computer, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, "The invention finds application, for example, to a single processor configured to process multiple threads, or processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors. Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the

mutex ordering mechanism.").

See below for the further limitations of claims 3, 4.

3. Referring to claim 2, Williams discloses generating a fault signal if said comparison is not equal (From line 64 of column 3, "If just two processing sets are used, or if following elimination of one or more faulty processing sets only two valid processing sets remain operable, a difference between the operation of the processing sets can signal faulty operation of one of the processing sets, although identification of which one of the processing sets is faulty can be a more complex task than simply employing majority voting.").

4. Further referring to claim 3, Williams discloses an input selectively enables or disables said comparing (From line 64 of column 3, "If just two processing sets are used, or if following elimination of one or more faulty processing sets only two valid processing sets remain operable, a difference between the operation of the processing sets can signal faulty operation of one of the processing sets, although identification of which one of the processing sets is faulty can be a more complex task than simply employing majority voting.").

5. Further referring to claim 4, Williams discloses said processing said thread on said second component is performed at a priority lower than a priority of said processing said thread on said first component (From line 35 of column 5, "The progress indication is used by the monitor to slow down a processor so that it does not become too far out of step with another. For this, processors also need to provide some way to allow the monitor to stall them.").

6. Referring to claim 5, Williams discloses said processing said thread on said second component occurs at a time delayed from that of said processing said thread on said first component (From line 35 of column 5, "The progress indication is used by the monitor to slow down a processor so that it does not become too far out of step with another. For this, processors also need to provide some way to allow the monitor to stall them.").

7. Referring to claim 23, Williams discloses a multiprocessor system executing a method of multithread processing on a computer, said method comprising: processing a thread on a first component, said first component capable of simultaneously executing at least two threads; processing said thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, "The invention finds application, for example, to a single processor configured to process multiple threads, or processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors. Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for

monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism.").

Further referring to claim 23, Williams discloses said processing said thread on said second component is performed at a priority lower than a priority of said processing said thread on said first component (From line 35 of column 5, "The progress indication is used by the monitor to slow down a processor so that it does not become too far out of step with another. For this, processors also need to provide some way to allow the monitor to stall them.").

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6499048 to Williams in view of US 5991900 to Garnett.** Referring to claim 3 Williams discloses a method of multithread processing on a computer, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, "The invention finds application, for example, to a single processor configured to process multiple

threads, or processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors. Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism.").

Although Williams does not specifically disclose the comparison step is bypassed by an input that performs one of enabling and disabling said comparing, this is known in the art. An example of this is shown by Garnett, from line 20 of column 15, "FIG. 18 illustrates an alternative arrangement where the disable signal 137 is negated and is used to control a gate 131 at the output of the comparator 130. When the disable signal is active the output of the comparator is disabled, whereas when the disable signal is inactive the output of the comparator is enabled." A person of ordinary skill in the art at the time of the invention would have been motivated to selectively disable and enable comparison because, from line 47 of column 10 of Garnett, "After initial resetting on powering up the bridge, or following an out-of sync event, the bridge is in this initial EState 152. ... In this state, the individual processing sets 14 and 16 perform evaluations for determining a restart time. Each processing set 14 and 16 will determine its own restart timer timing. The timer setting depends on a "blame" factor for

the transition to the EState. A processing set which determines that it is likely to have caused the error sets a long time for the timer. A processing set which thinks it unlikely to have caused the error sets a short time for the timer. The first processing set 14 and 16 which times out, becomes a primary processing set. Accordingly, when this is determined, the bridge moves (153) to the primary EState 154. When either processing set 14/16 has become the primary processing set, the bridge is then operating in the primary EState 154. This state allows the primary processing set to write to bridge registers (specifically the SRRs 118)." and further from line 38 of column 4 of Williams, "If the monitor unit knows that the I/O operation will not change the state of the I/O system--a read without side effects, for example--it can pass the I/O operation as soon as the first I/O operation output from the fastest compared processing set arrives, to enhance operating speed. Even if, in a fault tolerant processing environment, the system eventually decides that the cycle was a mistake, it will have done no harm, and the optimization could speed things up."

10. **Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6499048 to Williams.** Referring to claim 24, Williams discloses a medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus (From the abstract, "A program controlled apparatus...") to perform a method of multithread processing, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a

result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, "The invention finds application, for example, to a single processor configured to process multiple threads, or processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors. Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism."). Although Williams does not specifically disclose this medium can be an Application Specific Integrated Circuit (ASIC), using an ASIC to implement a method is notoriously well known in the art. Examiner takes official notice for ASICs. A person of ordinary skill in the art at the time of the invention would have been motivated to implement a method because ASICs improve performance over general-purpose CPUs, because ASICs are "hardwired" to do a specific job and do not incur the overhead of fetching and interpreting stored instructions.

Further referring to claim 24, Williams discloses said processing said thread on said second component is performed at a priority lower than a priority of said processing said thread on said first component (From line 35 of column 5, "The progress indication is used by the monitor to slow down a processor so that it does not become too far out

of step with another. For this, processors also need to provide some way to allow the monitor to stall them.").

11. Referring to claim 25, Williams discloses a medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus (From the abstract, "A program controlled apparatus...") to perform a method of multithread processing, said method comprising: processing a first thread on a first component, said first component capable of simultaneously executing at least two threads; processing said first thread on a second component, said second component capable of simultaneously executing at least two threads; and comparing a result of said processing on said first component with a result of said processing on said second component (From line 3 of column 2, "The invention finds application, for example, to a single processor configured to process multiple threads, or processes concurrently. The processes could, for example, be operating system processes. The invention also finds application to a plurality of processing units, each configured to process at least one thread. A monitor unit can be connected to the processing units for monitoring equivalent operation of the processors. Each processing unit may be configured to process multiple threads concurrently. The invention also finds application to apparatus comprising a plurality of processing sets, where each processing set comprises a plurality of processors. A monitor unit can be provided for monitoring equivalent operation of the processing sets, the monitor unit comprising the mutex ordering mechanism."). Although Williams does not specifically disclose this medium can be a Read Only Memory (ROM), using a ROM to implement a method is notoriously well

known in the art. A person of ordinary skill in the art at the time of the invention would have been motivated to use a ROM because the person does not want the instructions to change and because ROM is non-volatile.

Further referring to claim 25, Williams discloses said processing said thread on said second component is performed at a priority lower than a priority of said processing said thread on said first component (From line 35 of column 5, "The progress indication is used by the monitor to slow down a processor so that it does not become too far out of step with another. For this, processors also need to provide some way to allow the monitor to stall them.").

Allowable Subject Matter

12. Claims 6-22 allowed.

Response to Arguments

13. Applicant's arguments filed 18 April 2005 have been fully considered but they are not persuasive. Regarding Applicant's argument (page 11 and 12) that Examiner does not give "priority" the plain meaning of the claim language, Examiner notes that Dictionary.com's definition of priority is

1. Precedence, especially established by order of importance or urgency.

2. 1. An established right to precedence. 2. An authoritative rating that establishes such precedence.

3. A preceding or coming earlier in time.

4. Something afforded or deserving prior attention.

Although Examiner does not, apparently, use Applicant's preferred meaning, Examiner

assures Applicant that both a broad and reasonable interpretation has been applied.

Indeed, from paragraph 28 of Applicant's pre-grant publication, "Hence, the higher priority (foreground) thread can proceed at (nearly) full speed, and the lower priority thread (background) will consume whatever resources are left over. It is noted that the foreground thread may occasionally be slowed down by the background thread, for example, when the background thread is already using a shared resource that the foreground thread needs."

Relative to claim 5 (page 13), Applicant argues that it is just as likely in Williams that the second processor will lag the first processor. As claimed, and as interpreted, this does not differentiate the claims from Williams. Applicant merely claims that a thread has priority (precedence). This does not cover all threads at all times. This applies equally to claims 4 and 23-25.

14. Regarding Applicant's argument (page 11) that Williams does a disabling from the point of view of graceful degradation whereas the Applicant's disabling allows different programs to be run on the processors when high throughput is needed, Examiner does indeed appreciate that disabling comparison can increase throughput, as does Williams, as indicated in the motivation in the combination of Williams in view of Garnett above.

Examiner's previous rejection, still present, however, indicates that Applicant does not appreciate that the claim language does not specifically limit it to Applicant's intended meaning. The Williams-Garnett rejection has been applied as a courtesy by Examiner to expedite prosecution.

15. Regarding Applicant's argument (page 13) that William does not teach a time delay between first and second components, Williams has specifically disclosed that one processor can operate at a higher speed than the other processor.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 5016249 to Hurst et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100